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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,734	10/06/2003	Sompong Paul Olarig	200303856-3	2861

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
SPITTLE, MATTHEW D	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/679,734	**Applicant(s)** OLARIG ET AL.
	Examiner Matthew D. Spittle	**Art Unit** 2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6,7,9,10,47 - 54* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1,2,4,6,7,9,10, 47 - 54* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *10/6/2003*.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 2, 4, and 47 - 49 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,675,248. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of the patent contains every limitation of claims 1, 2, 4, and 47 – 49 of the instant application.

* * *

Claims 6 and 7 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,674,248 in view of Horan et al. (5,892,964).

With regard to claim 6, claim 1 of U.S. Patent No. 6,675,248 recites a computer system with an AGP to AGP bridge connecting at least two AGP-compatible devices via a first AGP bus. The system of claim 1 differs from claim 6 in that it fails to disclose the first AGP bus acting as a first 32-bit AGP bus and a second 32-bit AGP bus; both capable of operating concurrently. Horan et al. ('964) teach two AGP buses able to operate concurrently, and also having the said buses adapted for connection to a single

64-bit wide data PCI device (column 13, lines 10 – 19). Horan et al. ('964) fail to explicitly teach a 64-bit AGP device, however, this would have been an obvious substitution to one of ordinary skill in this art since Horan et al. ('964) disclose that AGP and PCI devices may share the same AGP/PCI bus, controller, and arbiter of a core logic chipset used in a computer system (column 3, line 61 – column 4, line 2). It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to make the modification as described by Horan et al. ('964) to the computer system of Horan et al. ('238) in order to accommodate two AGP devices on an AGP/PCI device concurrently, as well as retain the ability to implement a 64-bit AGP device in the system.

With regard to claim 7, claim 1 of U.S. Patent No. 6,675,248 recites a computer system with an AGP to AGP bridge connecting at least two AGP-compatible devices via a first AGP bus, where the first bus may be 32-bit or 64-bit. The system of claim 1 differs from claim 7 in that it fails to disclose the said AGP to AGP bridge comprising an ASIC that interfaces with a core logic, said first AGP bus behaving as a superset of a standard 32-bit AGP bus. Horan et al. ('964) teach a core logic chip set which may be implemented as an ASIC and provides an AGP bus for two AGP devices (column 5, lines 26 – 38). In addition, Horan et al. ('964) teach two AGP buses able to be adapted for connection to a single 64-bide wide data PCI device (column 13, lines 10 – 19). Horan et al. ('964) fail to explicitly teach a 64-bit AGP bus, however, this would have been an obvious substitution to one of ordinary skill in this art since Horan et al. ('964) disclose that AGP and PCI devices may share the same AGP/PCI bus, controller, and arbiter of a core logic chipset used in a computer system (column 3, line 61 – column 4, line 2). It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to use an ASIC for implementing an AGP to AGP bridge since an ASIC is well known in the art to be used as a means for implementing bus bridges as evidenced by both Larson et al. (column 4, lines 4 – 8) and Riley et al. (column 2, lines 28 – 32).

Claims 9 and 10 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,674,248 in view of Horan et al. (5,892,964).

With regard to claim 9, claim 1 of U.S. Patent No. 6,675,248 recites a computer system comprising a central processing unit, a core logic connected to said central processing unit, a system random access memory connected to said core logic, a first AGP bus connected to said core logic, and an AGP to AGP bridge coupled to said core logic. The system of claim 1 differs from claim 9 in that it fails to disclose the said AGP to AGP bridge comprising a bus that is configured as two lower bit number buses, each of said lower bit number buses acting as a standard AGP bus to said core logic, each of said lower bit number buses operating concurrently with the other of said lower bit number bus. Horan et al. ('964) teach two 32-bit AGP buses able to operate concurrently, and also having the said buses adapted for connection to a single 64-bit wide data PCI device (column 13, lines 10 – 19). Horan et al. ('964) fail to explicitly teach a 64-bit AGP bus, however, this would have been an obvious substitution to one of ordinary skill in this art since Horan et al. ('964) disclose that AGP and PCI devices may share the same AGP/PCI bus, controller, and arbiter of a core logic chipset used in a computer system (column 3, line 61 – column 4, line 2). Therefore, examiner recognizes that two lower bit number AGP buses adapted to create a single larger bit number PCI bus may also be used to create a larger bit number AGP bus. It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to make the modification as described by Horan et al. ('964) to the computer system of Horan et al. ('238) in order to accommodate two AGP devices on an AGP/PCI device concurrently.

With regard to claim 10, claim 1 of U.S. Patent No. 6,675,248 recites the additional limitation of the AGP to AGP bridge having a PCI interface.

* * *

Claims 50 - 54 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,674,248 in view of Horan et al. (5,892,964), and further in view of Olarig (5,878,237).

With regard to claim 50, claim 1 of U.S. Patent No. 6,675,248 recites a computer system with an AGP to AGP bridge connecting at least two AGP-compatible devices via a first AGP bus. The system of claim 1 differs from claim 50 in that it fails to disclose the first AGP bus being a 64-bit bus performing as a first 32-bit AGP bus and a second 32-bit AGP bus, said first and second 32-bit AGP buses capable of operating concurrently. Horan et al. ('964) teach two AGP buses able to operate concurrently, and also having the said buses adapted for connection to a single 64-bit wide data PCI device (column 13, lines 10 – 19). Horan et al. ('964) fail to explicitly teach a 64-bit AGP device, however, this would have been an obvious substitution to one of ordinary skill in this art since Horan et al. ('964) disclose that AGP and PCI devices may share the same AGP/PCI bus, controller, and arbiter of a core logic chipset used in a computer system (column 3, line 61 – column 4, line 2). It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to make the modification as described by Horan et al. ('964) to the computer system of Horan et al. ('238) in order to accommodate two AGP devices on an AGP/PCI device concurrently, as well as retain the ability to implement a 64-bit AGP device in the system.

With regard to claim 51, claim 1 of U.S. Patent No. 6,675,248 recites a computer system with an AGP to AGP bridge connecting at least two AGP-compatible devices via a first AGP bus, where the first bus may be 32-bit or 64-bit. The system of claim 1 differs from claim 51 in that it fails to disclose the said AGP to AGP bridge comprising an ASIC that interfaces with a core logic, said first AGP bus behaving as a superset of a standard 32-bit AGP bus. Horan et al. ('964) teach a core logic chip set which may be implemented as an ASIC and provides an AGP bus for two AGP devices (column 5, lines 26 – 38). In addition, Horan et al. ('964) teach two AGP buses able to be adapted for connection to a single 64-bide wide data PCI device (column 13, lines 10 – 19). Horan et al. ('964) fail to explicitly teach a 64-bit AGP bus, however, this would have been an obvious substitution to one of ordinary skill in this art since Horan et al. ('964) disclose that AGP and PCI devices may share the same AGP/PCI bus, controller, and arbiter of a core logic chipset used in a computer system (column 3, line 61 – column 4, line 2). It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to use an ASIC for implementing an AGP to AGP bridge since an ASIC is well known in the art to be used as a means for implementing bus bridges as evidenced by both Larson et al. (column 4, lines 4 – 8) and Riley et al. (column 2, lines 28 – 32).

With regard to claim 52, claim 1 of U.S. Patent No. 6,675,248 recites a computer system comprising a central processing unit, a core logic connected to said central processing unit, a system random access memory connected to said core logic, a first AGP bus connected to said core logic, and means for bridging at least two AGP-compatible devices to said computer system via said first AGP bus. The system of claim 1 differs from claim 52 in that it fails to disclose a geometry processor and a rendering processor connected to said bridging means. Examiner notes that it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include a geometry processor and a rendering processor on an AGP bus for performing geometric processing and rendering in a computer graphics system, as evidenced by Deering (where a 3D graphics accelerator may be interpreted as a rendering or geometric processor; column 4, lines 3 – 11, 20 – 33) and Wilde (where a graphics processor may be interpreted as a rendering or geometric processor; Figure 3, item 120; column 5, lines 12 – 29; Figure 3, item 112).

With regard to claim 53, claim 1 of U.S. Patent No. 6,675,248 recites a computer system comprising a central processing unit, a core logic connected to said central processing unit, a system random access memory connected to said core logic, a first AGP bus connected to said core logic, and a means for bridging at least two AGP-compatible devices to said computer system via said first AGP bus. The system of claim 1 differs from claim 53 in that it fails to disclose a geometry processor and rendering processor which can communicate without using said core logic. Olarig ('237) teach using an input output processor (IOP) to perform peer-to-peer PCI transactions with other I/O PCI devices residing on the same or other PCI buses (column 7, lines 19 – 29; column 9, lines 32 – 44), but fails to teach AGP buses or devices. However, Horan et al. ('964) teach that AGP and PCI devices may share the same AGP/PCI bus, controller, and arbiter of a core logic chipset used in a computer system (column 3, line 61 – column 4, line 2). Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the system of Horan et al. ('238) to use the input output processor as taught by Olarig ('237) with an AGP bus and AGP devices substituted as taught by Horan et al. ('964) for the purpose of enabling the geometric processor and rendering processor to communicate without using the said core logic.

With regard to claim 54, Horan et al. ('964) implicitly teach the additional limitation of the said geometry processor and said rendering processor residing on a printed circuit board. Horan et al. ('964) teach using an AGP compliant device card in an AGP slot (column 8, lines 13 – 15, 47 – 48; column 15, lines 16 – 19). Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a geometry processor and rendering processor on a printed circuit board (interpreted as an AGP compliant device card) in order to provide for a means of physical attachment and electrical connectivity to the computer system as described by Horan et al. ('238).

Claim Objections

Claim 54 is objected to because of the following informalities: Claim 54 contains the misspelling of the word "processor." Appropriate correction is required.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/18/05